REMARKS

Claim Rejections Under 35 U.S.C. § 102

Claims 1-2 and 4 were rejected under 35 U.S.C. § 102(b) as being anticipated by *Hong* (U.S. Patent No. 5,414,287). Applicant respectfully traverses this rejection.

Claims 1, 7, and 11 have been amended to more distinctly claim the subject matter that Applicant regards as the invention. The wordline of the present invention is now more clearly claimed as being a separate structure from the control gates yet connected to the pair of control gates in each trench.

Hong discloses a method and structure for manufacturing a high-density, split gate flash memory cell. The Examiner states that the control gate 54 of *Hong* is the same as Applicant's wordline. However, Applicant's claims as amended are to a wordline structure that is formed separately from, yet connected to, the pair of control gates in each trench. *Hong* neither teaches nor suggests such a wordline structure as presently claimed.

Claim Rejections Under 35 U.S.C. § 103

Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Hong*, in view of *Kawata* (U.S. Patent No. 6,157,061). Claims 5-8 and 11-12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Hong* in view of *Noble et al.* (U.S. Patent No. 6,486,027). Claim 9 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Hong*, in view of *Noble et al.* and further in view of *Kawata*. Claim 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Hong*, in view of *Noble et al.*, as applied to claims 5-8 and 11-12 above, and further in view of *Mori* (U.S. Patent No. 5,071,782). Applicant respectfully traverses these rejections.

Kawata discloses a non-volatile semiconductor memory device that includes a vertical memory cell. However, *Kawata* neither teaches nor suggests Applicant's invention, as claimed in the amended claims, for a pair of control gates formed as a single unit in each trench and separated by a separate wordline structure.

Noble et al. discloses a method for forming high-density flash memory. However, *Noble et al.* neither teaches nor suggests Applicant's invention, as claimed in the amended claims, for a pair of control gates formed as a single unit in each trench and separated by a separate wordline structure.

Mori discloses a vertical memory cell EPROM array. However, *Mori* neither teaches nor suggests Applicant's invention, as claimed in the amended claims, for a pair of control gates formed as a single unit in each trench and separated by a separate wordline structure.

Even if it were obvious to combine *Hong*, *Noble et al.*, *Kawata*, and/or *Mori*, and Applicant maintains that it is not, the combination does not teach or suggest Applicant's invention as claimed in the amended claims. The cited references neither teach nor suggest, individually or together, a method for fabricating a memory array having a plurality of memory cells, each cell having a pair of control gates formed as a single unit in each trench and a separate wordline structure separating the pair of control gates.

CONCLUSION

For the above-cited reasons, Applicant respectfully requests that the Examiner allow the claims of the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

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